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L36	((ic or integrated) and coheren$5 and DRAM and controller$1 and chip and scalar and vector).clm.	0	L36
L35	((ic or integrarted) and coheren$5 and DRAM and controller$1 and chip and scalar and vector).clm.	0	L35
L34	L33	0	L34

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L33	((ic or integrarted) and coheren$5 and DRAM and I near1 O near3 controller$1 and chip and scalar and vector).clm.	0	L33

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L25	l10 and l13	62	L25
L24	l10 and l12	121	L24
L23	l9 and l15	1	L23
L22	l9 and l14	1	L22
L21	l9 and l13	26	L21
L20	l9 and l12	41	L20
L19	l5 and l15	2	L19
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L12	(712/2-300)[CCLS]	13531	L12
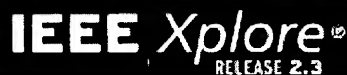
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Araki, T.; Toyokura, M.; Akiyama, T.; Takeno, H.; Wilson, B.; Aono, K.;
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Volume ii, 19-22 April 1994 Page(s):II/417 - II/420 vol.2
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